In the Claims

1.-21. (Cancelled)

22. (Previously Presented) A stud capacitor structure comprising:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein at least about one-third of the stud is embedded in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

23. (Original) The stud capacitor structure according to claim 22, the structure further including:

a seed film disposed above the first conductive plug, wherein the seed film is below and on the stud.

24. (Original) The stud capacitor structure according to claim 22, the structure further including:

a seed film disposed above the first conductive plug, wherein the seed film is below and on the stud, and wherein the seed film is embedded in the first dielectric stack.

25. (Original) The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud; and

a storage cell plate disposed over the storage cell dielectric film.

26. (Original) The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud, wherein the storage cell dielectric film has a thickness in a range from about 30 Å to about 80 Å.

27. (Original) The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud, wherein the storage cell dielectric film is selected from titanium oxide, tantalum oxide, aluminum oxide, strontium titanate, barium strontium titanate, lead titanate, lead lanthanum titanate, lead lanthanum zirconium tantalate, lead zirconium titanate, strontium bismuth tantalate, and combinations thereof.

28. (Original) The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud, wherein the storage cell dielectric film has a dielectric constant range from about 9 to about 300; and

a storage cell plate disposed over the storage cell dielectric film.

29. (Original) The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud; and

a storage cell plate disposed over the storage cell dielectric film, wherein the storage cell plate is selected from the same material as the stud, platinum, rhodium, ruthenium, iridium, palladium, nickel, combinations thereof, and an alloy.

30. (Original) The stud capacitor structure according to claim 22, the structure further including:

a storage cell dielectric film disposed over the stud; and

a storage cell plate disposed over the storage cell dielectric film, wherein the storage cell plate is a different material from the stud, selected from a metal nitride, titanium nitride, tantalum nitride, and tungsten nitride.

31. (Original) The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below.

32. (Original) The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below, wherein the barrier structure is disposed above a polysilicon plug.

33. (Original) The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below, wherein the barrier structure is disposed above a tungsten plug.

34. (Original) The stud capacitor structure according to claim 22, the structure further including:

a barrier structure disposed between and in contact with the stud above and the first conductive plug below, wherein the barrier structure is disposed above and on the first conductive plug.

35. (Previously Presented) A storage cell comprising:

a platinum electrode comprising a platinum seed layer and a platinum stud, the platinum electrode being partially embedded in a first dielectric stack, wherein the platinum stud is above and on a platinum seed film;

a first conductive plug disposed below the platinum seed film;

a barrier structure disposed between the platinum seed film and the first conductive plug;

a tantalum oxide dielectric film disposed over the platinum stud; and

a platinum cell plate disposed over the tantalum oxide dielectric film.

36. (Currently Amended) The storage cell according to claim 35, wherein the barrier structure further includes:

a metal silicide first barrier film disposed above and on the first conductive plug; and

a refractory metal nitride second barrier film disposed above and on the ~~metalsilicide~~ metal silicide first barrier film.

37. (Original) The storage cell according to claim 35, wherein the barrier structure is disposed above and on a polysilicon first conductive plug.

38. (Original) The storage cell according to claim 35, wherein the barrier structure is disposed above and on a tungsten first conductive plug.

39. (Original) The storage cell according to claim 35, wherein the barrier structure is disposed above and on the first conductive plug, wherein the first conductive plug is selected from polysilicon and tungsten.

40. (Original) The storage cell according to claim 35, wherein the tantalum oxide dielectric film has a thickness in a range from about 30 Å to about 80 Å.

41. (Original) An electrical device comprising:

a storage cell stud partially embedded in a first dielectric stack, wherein the storage cell stud extends into an upper dielectric stack that is disposed above and on the first dielectric stack;

a seed film disposed against the storage cell stud, wherein the seed film is disposed in a contact corridor in the first dielectric stack; and

a protective film remnant disposed on an upper surface of the first dielectric stack, wherein the protective film remnant is disposed between the first dielectric stack and a portion of the seed film.

42. (Original) The electrical device according to claim 41, the electrical device further including:

a storage cell dielectric film disposed above the storage cell stud; and

a storage cell plate disposed above the storage cell dielectric film.

43. (Original) The electrical device according to claim 41, the electrical device further including:

a storage cell dielectric film disposed above the storage cell stud, wherein the storage cell dielectric film has a thickness in a range from about 30 Å to about 80 Å; and

a storage cell plate disposed above the storage cell dielectric film.

44. (Original) The electrical device according to claim 41, the electrical device further including:

a storage cell dielectric film disposed above the storage cell stud, wherein the storage cell dielectric film has a dielectric constant range from about 9 to about 300; and

a storage cell plate disposed above the storage cell dielectric film.

45. (Original) The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package.

46. (Original) The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package; and

a host, wherein the chip package is disposed in the host.

47. (Original) The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package; and

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module.

48. (Original) The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package; and

a host, wherein the chip package is disposed in the host, wherein the host includes a memory module; and

an electronic system, wherein the memory module is disposed in the electronic system.

49. (Original) The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package;

a host, wherein the chip package is disposed in the host, wherein the host includes a dynamic random access memory module; and

an electronic system, wherein the dynamic random access memory module is disposed in the electronic system.

50. (Original) The electrical device according to claim 41, wherein the electrical device further includes:

a chip package, wherein the storage cell stud is disposed in the chip package;

a host, wherein the chip package is disposed in the host; and

an electronic system, wherein the host is disposed in the electronic system.

51. (Previously Presented) An electronic system, comprising:

a circuit module;

a user interface; and

a stud capacitor structure disposed in the circuit module or the user interface, the storage cell stud including:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded to about 30% of its height in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

52. (Original) The electronic system according to claim 51, wherein the user interface includes at least one of a keyboard, a pointing device, a monitor, a printer, a tuning dial, a display and speakers of a radio, an automobile ignition switch, an automobile gas pedal, a card reader, a keypad, and an automated teller machine.

53. (Original) The electronic system according to claim 51, wherein the circuit module includes a single integrated circuit.

54. (Previously Presented) A memory system, comprising:

a memory device;

a memory controller;

an external system bus; and

a command link; and

a stud capacitor structure disposed in the circuit module or the user interface, the storage cell stud including:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded to about 30% of its height in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

55. (Original) The memory system according to claim 54, wherein the memory system is selected from one of DIMM DRAM, a SIMM DRAM, a DIMM SDRAM, a SIMM SDRAM, a DIMM DDRAM, and a SIMM DDRAM.

56. (Previously Presented) A computer system, comprising:

a processor;

a memory system coupled to the processor;

an input/output (I/O) circuit coupled to the processor and the memory system; and

a stud capacitor structure disposed in the processor or the memory system, the storage cell stud including:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded to about 30% of its height in a first dielectric stack; and

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack.

57. (Original) The computer system according to claim 56, wherein the processor is disposed in a host selected from a clock, a television, a cell phone, a personal computer, an automobile, an industrial control system, an aircraft, and a hand-held.

58. (Original) The computer system according to claim 56, wherein the memory system is selected from a DIMM DRAM, a SIMM DRAM, a DIMM SDRAM, a SIMM SDRAM, a DIMM DDRAM, and a SIMM DDRAM, and wherein the computer system is selected from a personal computer, a server, and a network computer.

59. (Previously Presented) A stud capacitor structure comprising:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded in a first dielectric stack;

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack; and

a seed film disposed above the first conductive plug, wherein the seed film is below and on the stud.

60. (Previously Presented) The stud capacitor structure of claim 59, wherein the stud includes a bottom portion having a first width and a top portion having a second width greater than the first width.

61. (Previously Presented) The stud capacitor structure of claim 60, wherein the bottom portion extends into the first dielectric stack.

62. (Previously Presented) The stud capacitor structure of claim 61, wherein the top portion extends into the upper dielectric stack.

63. (Previously Presented) A stud capacitor structure comprising:

a first conductive plug disposed above a substrate;

a stud coupled to the first conductive plug, wherein the stud is partially embedded in a first dielectric stack;

an upper dielectric stack disposed above the first dielectric stack, wherein the stud extends into the upper dielectric stack; and

a seed film disposed above the first conductive plug, wherein the seed film is below and on the stud, and wherein the seed film is partially embedded in the first dielectric stack.

64. (Previously Presented) The stud capacitor structure of claim 63, wherein the stud includes a bottom portion having a first width and a top portion having a second width greater than the first width.

65. (Previously Presented) The stud capacitor structure of claim 64, wherein the bottom portion extends into the first dielectric stack.

66. (Previously Presented) The stud capacitor structure of claim 65, wherein the top portion extends into the upper dielectric stack.

67. (Previously Presented) The stud capacitor structure of claim 22, wherein the stud includes a bottom portion and a top portion, wherein the top portion is wider than the bottom portion.

68. (Previously Presented) The stud capacitor structure of claim 67, wherein the bottom portion extends into the first dielectric stack.

69. (Previously Presented) The stud capacitor structure of claim 68, wherein the top portion extends into the upper dielectric stack.

70. (Previously Presented) The storage cell of claim 35, wherein the stud extends into an upper dielectric stack that is disposed above the first dielectric stack.

71. (Previously Presented) The storage cell of claim 35, wherein the stud extends above the first dielectric stack.

72. (Previously Presented) The storage cell of claim 35, wherein the first dielectric stack includes a protective film remnant that is disposed adjacent a portion of the seed film.

73. (Previously Presented) The electric system of claim 51, wherein the stud includes a bottom portion having a first width and a top portion having a second width greater than the first width.

74. (Previously Presented) The electric system of claim 73, wherein the bottom portion extends into the first dielectric stack.

75. (Previously Presented) The electric system of claim 74, wherein the top portion extends into the upper dielectric stack.

76. (Currently Amended) The electric system of claim 51, wherein the stud capacitor structure includes a protective film remnant that is part of the first dielectric stack.

77. (Previously Presented) The electric system of claim 51, wherein the structure includes a seed film disposed above the first conductive plug.

78. (Previously Presented) The electric system of claim 77, wherein the seed film includes platinum.

79. (Previously Presented) The electric system of claim 77, wherein the seed film includes a portion embedded in the first dielectric stack.

80. (Currently Amended) The structure of claim 22, wherein the stud has a height and about ~~on-third~~ one-third of the height is in the first dielectric stack.

81. (Previously Presented) The structure of claim 22, wherein the stud extends into the first dielectric stack in a range of about 100 angstroms to about 3,000 angstroms.

82. (Previously Presented) The structure of claim 22, wherein the stud extends into the first dielectric stack in a range of about 200 angstroms to about 2,500 angstroms.

83. (Previously Presented) The structure of claim 22, wherein the stud extends into the first dielectric stack in a range of about 500 angstroms to about 2,000 angstroms.

84. (Previously Presented) The structure of claim 22, wherein the stud extends in a vertical dimension that is significantly greater than the horizontal dimension.

85. (Previously Presented) The storage cell of claim 35, wherein the platinum stud has a height and about one-third of the height is in the first dielectric stack.

86. (Previously Presented) The storage cell of claim 35, wherein the platinum stud has a height and about one-third of the height is in the first dielectric stack.

87. (Previously Presented) The storage cell of claim 35, wherein the platinum stud extends into the first dielectric stack in a range of about 100 angstroms to about 3,000 angstroms.

NOR 7/25/06 88 ~~89~~. (Previously Presented) The storage cell of claim 35, wherein the platinum stud extends into the first dielectric stack in a range of about 200 angstroms to about 2,500 angstroms.

NOR 7/26/06 89 ~~90~~. (Previously Presented) The storage cell of claim 35, wherein the platinum stud extends into the first dielectric stack in a range of about 500 angstroms to about 2,000 angstroms.

NOR 7/26/06 90 91. (Previously Presented) The storage cell of claim 35, wherein the platinum stud extends in a vertical dimension that is significantly greater than the horizontal dimension.